REMARKS

The applicants hereby provisionally elect Group I. Claims 1-18 and 22-23 read upon the elected group.

This amendment/election is in response to the Office Action mailed 05/29/2007 in regard to the above-identified patent application. Claims 19-21 have been deleted above, without prejudice, in response to the election/restriction requirement. Claims 1-18 and 22-23 are now pending in this case. A separate sheet showing the status of all claims, in accordance with C.F.R. 121 is enclosed

Should any unresolved issue remain, the Examiner is invited to call Applicant's Attorney at the telephone number indicated below.

Respectfully submitted,

/Kevin P. Correll/ 06/21/07

Kevin P. Correll (Reg. No. 46,641) Date

K. P. Correll & Associates, LLP
270 Bellevue Ave, #326
Newport, RI 02840
V: (401) 295-7377
F: (401) 295-9054

Claim Amendments

1. (Previously presented) A phase division multiple access (PDMA) system, the system comprising:

at least one receiver logic combiner, the at least one receiver logic combiner adapted to generate a plurality of composite PN codes, wherein each of the plurality of composite PN codes are separated by a predetermined PN phase.

2. (Previously presented) A PDMA system as in claim 1, further comprising at least three first receiver pseudo-noise (PN) component code generators coupled to the at least one receiver logic combiner, wherein each of the at least three first receiver pseudo-noise (PN) component code generators generate relatively prime PN component codes.

3. (Previously presented) A PDMA system as in claim 2 further comprising at least one PN phase delayer coupled to one of the at least three first receiver PN component code generators.

4. (Previously presented) A PDMA system as in claim 2 wherein the at least three first receiver pseudo-noise (PN) component code generators comprise four first receiver PN component code generators.

5. (Previously presented) A PDMA system as in claim 1 wherein the predetermined PN phase substantially equals at least one PN minor epoch.

6. (Previously presented) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MAND logic combiner.

7. (Previously presented) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MAJ logic combiner.

8. (Previously presented) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MOD logic combiner.

9. (Previously presented) A method for generating multi-phase composite pseudo-noise (PN) codes, the method comprising:

generating a first composite PN code; and

generating a second composite PN code, wherein the second composite code is PN phase separated from the first composite PN code.

10. (Previously presented) A method as in claim 9 wherein generating the first composite PN code comprises:

generating a plurality of relatively prime PN component codes;

PN phase delaying one of the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

11. (Previously presented) A method as in claim 10 wherein generating the second composite PN code comprises:

generating the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

12. (Previously presented) A method as in claim 9 wherein generating the second composite PN code further comprises generating the second composite PN code at least one PN minor epoch phase separated from the first composite PN code.

13. (Previously presented) A method as in claim 10 wherein combining the plurality of relatively prime PN component codes further comprises MOD combining the plurality of relatively prime PN component codes.

14. (Previously presented) A method as in claim 10 wherein combining the plurality of relatively prime PN component codes further comprises MAJ combining the plurality of relatively prime PN component codes.

15. (Previously presented) A method as in claim 10 wherein combining the plurality of relatively prime PN component codes further comprises MAND combining the plurality of relatively prime PN component codes.

16. (Previously presented) A method as in claim 11 wherein combining the plurality of relatively prime PN component codes further comprises MOD combining the plurality of relatively prime PN component codes.

17. (Previously presented) A method as in claim 11 wherein combining the plurality of relatively prime PN component codes further comprises MAJ combining the plurality of relatively prime PN component codes.

18. (Previously presented) A method as in claim 11 wherein combining the plurality of relatively prime PN component codes

further comprises MAND combining the plurality of relatively prime PN component codes.

19. (Cancel

20. (Cancel)

21. (Cancel)

22. (Previously presented) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes, the method comprising:

generating a first composite PN code, wherein generating the first composite PN code comprises:

generating a plurality of relatively prime PN component codes;

combining the plurality of relatively prime PN component codes;

generating a second composite PN code, wherein the second composite code is PN phase separated from the first composite PN code wherein generating the second composite PN code comprises:

generating the plurality of relatively prime PN component codes;

PN phase delaying one of the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

23. (Previously presented) A program storage device as in claim 22 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.